What is claimed is:

[Claim 1] Method of forming an interconnect structure comprising the steps of:

depositing a dielectric layer;
forming a hard mask over the dielectric material;
etching trenches in the dielectric material;
depositing a liner material over the hard mask and within the trenches; and
overfilling the trenches with a conductive material;
characterized by:
performing a first chemical mechanical polishing process to remove conductive material which is atop the liner, thereby exposing the liner;
removing that portion of the liner which is atop the hard mask;
removing a first portion of the hard mask using a wet etch process, thereby leaving in place a second portion of the hard mask; and
performing a touch-up polishing process to remove conductive material and liner material protruding from the trenches.

[Claim 2] The method of claim 1, wherein the dielectric layer comprises a low-k material.

[Claim 3] The method of claim 1, wherein the dielectric layer comprises an ultralow-k material.

[Claim 4] The method of claim 1, wherein the hard mask comprises:

a layer of silicon carbide material atop the dielectric layer; and
a layer of oxide atop the layer of silicon carbide.

[Claim 5] The method of claim 1, wherein the conductive material is copper.

[Claim 6] The method of claim 1, wherein the portion of the liner which is atop the hard mask is removed by a reactive ion etch (RIE) or a Gas Cluster Ion Beam (GCIB) process.

[Claim 7] The method of claim 1, wherein the portion of the liner which is atop the hard mask is removed by a second chemical mechanical polishing process.

[Claim 8] The method of claim 1, wherein the first portion of the hard mask comprises oxide.

[Claim 9] The method of claim 8, further comprising the step of:

ensuring that the oxide portion of the hard mask is thick enough such that the topographical variations after the first chemical mechanical polishing process and liner removal are entirely within the oxide portion of the hard mask.

[Claim 10] The method of claim 8, wherein the oxide has a thickness in the range of 50 - 5000 Å.

[Claim 11] The method of claim 1, wherein the second portion of the hard mask comprises a silicon carbide (SiC) material.

[Claim 12] The method of claim 1, wherein:

the first portion of the hard mask comprises oxide; and
the second portion of the hard mask comprises a silicon carbide (SiC) material.

[Claim 13] The method of claim 1, wherein the touch-up polishing process uses an abrasive-free or low-abrasive polish to obtain a very high selectivity between the conductive material and the second portion of the hard mask.

[Claim 14] Method of forming an interconnect structure comprising the steps of:

depositing a dielectric material;
forming a hard mask over the dielectric material;
etching trenches in the dielectric material; and
overfilling the trenches with a conductive material;
characterized by:
performing a first chemical mechanical polishing step;
then, performing a wet etch step; and
then, performing a second chemical mechanical polishing step.

[Claim 15] The method of claim 14, wherein at least a portion of the hard mask is left substantially intact.

[Claim 16] The method of claim 14, wherein the portion of the hard mask which is left substantially intact comprises a silicon carbide SiC material.

[Claim 17] A semiconductor device comprising an interconnect structure, the interconnect structure comprising:

an interlevel dielectric layer (ILD) layer having trenches filled with conductive material;
a hard mask overlying the interlevel dielectric layer (ILD); and
wherein at least a portion of the hard mask overlying the interlevel dielectric layer is substantially uniform in thickness and substantially planar irrespective of pattern density variations.

[Claim 18] The semiconductor device of claim 17, wherein the conductive material is copper.

[Claim 19] The semiconductor device of claim 17, wherein the portion of the hard mask comprises a silicon carbide (SiC) material.

[Claim 20] The semiconductor device of claim 17, wherein:

the trenches are first overfilled with conductive material; and
processes used to remove excess conductive material substantially do not affect the portion of the hard mask overlying the interlevel dielectric layer.